REMARKS

Applicant thanks Examiner Sarkar for the telephonic interview on August 13, 2002. Although, a consensus regarding the allowance of claims was not achieved, Applicant has incorporated the Examiner's comments and suggestions in this amendment.

Objection

Claim 26 was objected to for containing the word "silicone" instead of "silicon. Applicant has amended Claim 26 correcting the typographical error. Accordingly, Applicant respectfully requests the withdrawal of the objection of Claim 26.

Rejection Under 35 U.S.C. §102(e)

Claims 24-29, 31, 35-38, 40, 41 and 46-48 were rejected under 35 U.S.C. §102(e) as being anticipated by Henley (U.S. Patent 6,083,324).

Claim 24

In regards to Claim 24, the Henley reference does not disclose or teach "a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material" as is disclosed and claimed in Claim 24 of the present application. Moreover, Applicant has amended Claim 24 to further define and clarify the patentability of the present invention over the Henely reference. The amendments clarify that the second layer is an **undamaged** layer of moncrystalline semiconductor material. That is, the second layer is undamaged because the ions implanted to form the gettering zone are implanted through the first layer not the second layer. As explained in the application on page 5, lines 30-31 of the present application, ion implantation into a semiconductor layer results in the formation of an amorphorus semiconductor layer. Unlike the prior art, the first layer is bonded to the bond oxide and the second layer is then used as a device layer in forming semiconductor devices. See, Figures 2A-4 of the present

application. By using the second undamaged layer as a device layer instead of the first layer, semiconductor devices of relatively high quality are formed. The Henely reference does not disclose or teach a second layer of undamaged monocrystalline semiconductor material as is disclosed and claimed in Claim 24 of the present application.

In view of the forgoing, Claim 24 is patentably distinct from the Henley reference. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 24 under 35 U.S.C § 102. Furthermore, since Claim 25 depends from and further defines patentably distinct Claim 24, Applicant believes this claim is also allowable and respectfully requests the withdrawal of the rejection of Claim 25.

Claim 26

In regards to claim 26, the aforementioned arguments that apply to Claim 24 also applies to Claim 26. In particular, that the Henley reference does not disclose or teach a second layer of undamaged monocrystaline semiconductor material and then bonding the first layer to a handle wafer as is disclosed and claimed in Claim 26 of the present application.

In view of the forgoing, Claim 26 is patentably distinct from the Henley reference. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 26 under 35 U.S.C § 102. Furthermore, since Claim 27 depends from and further defines patentably distinct Claim 26, Applicant believes this claim is also allowable and respectfully requests the withdrawal of the rejection of Claim 27.

Claim 28

In regards to claim 28, the aforementioned arguments that apply to Claims 24 and 26 also applies to Claim 28. In particular, that the Henley reference does not disclose or teach a semiconductor substrate with a second layer of undamaged mononcrystalline semiconductor material and an insulating bond layer deposited on a first layer mononcrystalline semiconductor material as is disclosed and claimed in Claim 28 of the present application.

In view of the forgoing, Claim 28 is patentably distinct from the Henley reference. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 28 under

35 U.S.C § 102. Furthermore, since Claims 29-37 depend from and further define patentably distinct Claim 28, Applicant believes these claims are also allowable and respectfully requests the withdrawal of the rejection of Claims 29-37.

Claim 38

In regards to Claim 38, the aforementioned arguments that apply to Claims 24, 26 and 28 also applies to Claim 38. In particular, that the Henley reference does not disclose or teach a bonded semiconductor-on-insulator substrate for an integrated circuit having a second layer of undamaged monocrystalline semiconductor material, a first layer of monocrystalline semiconductor material adjacent a first surface of substrate and an insulting bond layer disposited on the first surface of the substrate as is disclosed and claimed in Claim 38 of the present application.

In view of the forgoing, Claim 38 is patentably distinct from the Henley reference. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 38 under 35 U.S.C § 102. Furthermore, since Claims 39-48 depend from and further define patentably distinct Claim 38, Applicant believes these claims are also allowable and respectfully requests the withdrawal of the rejection of Claims 39-48.

Rejection Under 35 U.S.C. §103(a)

Claims 30 and 39 were rejected under 35 U.S.C. §103(a) as being unpatentable over Henley in view of Hori (U.S. Patent 5,731,637).

In regards to Claims 30 and 39, Applicant has amended claims 30 and 39. As amended neither Henely nor Hori alone or in combination suggest the combination or modification to arrive at what is claimed in dependant Claims 30 and 39 and their respective independent claims.

Claims 32-34 and 42-45 were rejected under 35 U.S.C. §103(a) as being unpatentable over Henley. Claim 45 has been cancel because it is a duplicate of claim 42.

In regards to Claims 32-34 and 42-44, the Henley reference, alone or combination, does not teach or suggest what is claimed in dependant claims 32-34 and 42-45 and their respective independent claims. In particular, the Henley reference, alone or in combination, does not teach or suggest a first layer of monocrystalline semiconductor material with a thickness of about 0.1 μm to about 0.8 μm as is disclosed and claimed in claims 32 and 42 of the present application. Moreover, the Henley reference, alone or in combination, does not teach or suggest a second layer of monocystalline semiconductor material with a thickness of about 0.2 μm to about 20 μm as is disclosed and claimed in claims 33 and 43. In addition, the Henley reference, alone or in combination, does not teach or suggest a gettering zone with a thickness of about 0.05 μm to about 0.2 μm as is disclosed and claimed in claims 34 and 44.

CONCLUSION

Claims 24, 26, 28, 30, 38, 39, 40 and 46 are amended. Claim 45 is canceled. Claims 49-56 are withdrawn from consideration. Claims 24-44 and 46-56 are currently pending in this application. Applicant respectfully submits that claims 24-44 and 46-48 are in condition for allowance and notification to that effect is earnestly requested. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2206.

If necessary, please charge and additional fees or credit overpayment to Deposit Account No. 501373.

Respectfully submitted,

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MARKED UP VERSION SHOWING CHANGES MADE

IN THE TITLE

"BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A [PLANER] PLANAR INTRINSIC GETTERING ZONE"

IN THE CLAIMS

24. (amended Twice) A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a [first] second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a [second] first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a

substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of undamaged monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer[,]; and

wherein the said semiconductor device is formed on said epitaxial layer.

26. (Amended Twice) A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a [first] second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a [second] first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth between the first layer of monocrystalline semiconductor material and the second layer of undamaged monocrystalline semiconductor material;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer adjacent the first layer of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline

semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise [silicone] silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

forming a semiconductor device on said bonded substrate.

28. (Amended Once) A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a mononcrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocystalline semiconductor material adjacent to said first surface and a second layer of undamaged [the] monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said [second] first surface of said wafer; and

a handle wafer bonded to said insulting bond layer.

30. (Amended Twice) The substrate of claim 28 wherein the monocrystalline semiconductor material comprises silicon and the substantially planer intrinsic gettering zone is formed by implanting ions of silicon through the first layer of monocrystalline semiconductor material [said implanted ions comprise silicon ions].

38. (Amended Once) A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially [planer] planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the [second] first surface of the wafer.

39. (Amended Once) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein [the first and second monocrystalline semiconductor material comprises silicon implanted by silicon ions] the first and second layers of monocrystalline semiconductor comprises silicon and the ions implanted through the first layer are silicon ions.

40. (Amended Once) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of undamaged monocrystalline semiconductor material is a device layer upon which semiconductor devices are formed. [further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer of monocrystalline semiconductor material].

45. Canceled

46. (Amended Once) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the [first] second layer.